Scheme of Instruction, Examination

(with effect from the academic year 2021-2022)

M.E. I to IV Semester

of

Two Year Post Graduate Degree Programme

in

Electronics & Communication Engineering

Specialization in

EMBEDDED SYSTEMS AND VLSI DESIGN

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Maturi Venkata Subba Rao (MVSR) Engineering College
Nadergul, Hyderabad - 501510
(Sponsored by Matrusri Education Society, Estd. 1980)
ISO 9001:2015 Certified Institution

(An Autonomous Institution)

Accredited by NAAC & NBA

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2021

Maturi Venkata Subba Rao (MVSR) Engineering College
Department of Electronics and Communication Engineering

SCHEME of INSTRUCTION & EXAMINTATION
M.E. (Electronics and Communication Engineering)
Specialization in Embedded Systems and VLSI Design

SEMESTER-I

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
1	P21PC001EC	Embedded System Design	3	1	-	4	30	70	3	4
2	P21PC002EC	Digital IC Design	3	-	-	3	30	70	3	3
3	Elective	Professional Elective – I	3	-	-	3	30	70	3	3
4	Elective	Professional Elective – II	3	-	-	3	30	70	3	3
5	P 21MC001CS	Research Methodology & IPR	3	-	-	3	30	70	3	3
6	Audit	Audit Course-I	2	-	-	2	30	70	3	0
Practical/ Laboratory Courses										
7	P21PC801EC	Embedded Systems Lab	-	-	2	2	50	-	3	1
8	P21PC802EC	Digital IC Design Lab	-	-	2	2	50	-	3	1
Total			**17**	**01**	**04**	**22**	**280**	**420**	**24**	**18**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:
1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester and the Open Elective course is offered in III-semester.

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SEMESTER-II

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	P21PC003EC	Real Time Operating System for Embedded System	3	1	-	4	30	70	3	4
2	P21PC004EC	Analog and Mixed Signal IC Design	3	1	-	4	30	70	3	4
3	Elective	Professional Elective – III	3	-	-	3	30	70	3	3
4	Elective	Professional Elective – IV	3	-	-	3	30	70	3	3
5	Audit	Audit Course – II	2	-	-	2	30	70	3	0
Practical/ Laboratory Courses										
6	P21PC803EC	Real Time Operating Systems Lab	-	-	2	2	50	-	3	1
7	P21PC804EC	Analog Mixed Signal IC Design Lab	-	-	2	2	50	-	3	1
8	P21PC805EC	Mini Project with Seminar	-	-	4	4	50	-	3	2
Total			**14**	**02**	**8**	**24**	**300**	**350**	**24**	**18**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:
1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester and the Open Elective course is offered in III-semester.

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SEMESTER-III

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	Elective	Professional Elective – V	3	-	-	3	30	70	3	3
2	OE	Open Elective	3	-	-	3	30	70	3	3
3	P21PW801EC	Major Project Phase – I	-	-	20	20	100	-	-	10
Total			**6**	**-**	**20**	**26**	**160**	**140**		**16**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester and the Open Elective course is offered in III-semester.

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SEMESTER-IV

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	P21PW802EC	Major Project Phase II (Dissertation)	-	-	32	32	-	200	-	16
Total			**-**	**-**	**32**	**32**	**-**	**200**	**-**	**16**

PC: Program Core **PE:** Professional Elective **OE**: Open Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester and the Open Elective course is offered in III-semester.

List of Subjects of Program Core

S. No.	Course Code	Course Title
1	P 21PC001EC	Embedded System Design
2	P 21PC002EC	Digital IC Design
3	P 21PC003EC	Real Time Operating System for Embedded System
4	P 21PC004EC	Analog and Mixed Signal IC Design

List of subjects for Professional Elective I

S. No.	Course Code	Course Title
1	P21PE001EC	Software for Embedded Systems
2	P21PE002EC	Hardware Software Co-Design
3	P21PE003EC	Reconfigurable Computing Systems
4	P21PE004EC	Advance Computer Architecture

List of subjects for Professional Elective II

S. No.	Course Code	Course Title
1	P21PE005EC	Low Power VLSI Design
2	P21PE006EC	Semiconductor Device Modeling
3	P21PE007EC	System on Chip Design
4	P21PE008EC	VLSI for Signal Processing

List of subjects for Professional Elective III

S. No.	Course Code	Course Title
1	P21PE009EC	Internet of Things
2	P21PE010EC	Network Embedded Applications
3	P21PE011EC	Embedded System design using ARM processors
4	P21PE012EC	Distributed Embedded Computing

List of subjects for Professional Elective IV

S. No.	Course Code	Course Title
1	P21PE013EC	System Verilog
2	P21PE014EC	Multi gate MOSFET Technology
3	P21PE015EC	VLSI Testing
4	P21PE016EC	VLSI Physical Design

List of subjects for Professional Elective V

S.No.	Course Code	Course Title
1	P21PE017EC	MEMS
2	P21PE018EC	Embedded Bio Medical Applications
3	P21PE019EC	VLSI Architectures
4	P21PE020EC	Machine Learning with Artificial Neural Networks

Mandatory Course

S. No.	Course Code	Course Title
1	P21MC001CS	Research Methodology & IPR

List of Open Electives

S. No.	Course Code	Course Title
1	P21OE001CE	Cost Management of Engineering Projects
2	P21OE002 CS	Business Analytics
3	P21OE003EC**	Fundamentals of Embedded System Design
4	P21OE004 EE	Waste to Energy
5	P21OE005ME	Industrial Safety

Note: ** Open Elective Subject is not offered to the students of ECE Department.

List of subjects of Audit Course-I

S. No.	Course Code	Course Title
1	P21AD001 HS	English for Academic and Research Writing
2	P21AD002 CE	Disaster Management
3	P21AD003 HS	Sanskrit for Technical Knowledge
4	P21AD004 HS	Value Education

List of subjects of Audit Course-II

S. No.	Course Code	Course Title
1	P21AD005 HS	Constitution of India and Fundamental Rights
2	P21AD006HS	Pedagogy Studies
3	P21AD007HS	Stress Management by Yoga
4	P21AD008 HS	Personality Development through Life Enlightenment Skills

List of Laboratory Courses

S. No.	Course Code	Course Title
1	P21PC801EC	Embedded Systems Design Lab
2	P21PC802EC	Digital IC Design Lab
3	P21PC803EC	Real Time Operating Systems Lab
4	P21PC804EC	Analog Mixed Signal IC Design Lab

List of Projects and Seminars

S. No.	Course Code	Course Title
1	P21PC805EC	Mini Project with Seminar
2	P21PW801EC	Major Project Phase – I
3	P21PW802EC	Major Project Phase – II (Dissertation)

Course Code	Course Title						Core/ Elective
P21PC001EC	Embedded System Design						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	1	-	-	30	70	4

Course Objectives

1. Describe the categories, applications, architecture and tools used in Embedded Systems and familiarize with ARM architecture.
2. Illustrate the architecture of ARM CORTEX –M3.
3. Explain programming with Cortex-M3/M4.
4. Analyze the Cortex-M4 Microcontroller architecture**.**
5. Discuss various serial Bus Communication Protocols used in Embedded Systems.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the categories, applications, architecture and tools used in Embedded Systems and familiarize with ARM architecture.
2. Understand the architecture of Cortex-M3.
3. Develop the skills to program Cortex-M3/M4.
4. Understand the architecture of Cortex-M4.
5. Analyze and use various serial, parallel and network busses used in Embedded Systems.

MODULE I

Embedded Concepts: Introduction to Embedded Systems, Application Areas, Categories of Embedded Systems, Overview of Embedded System architecture, Characteristics of embedded Systems, recent trends in embedded systems, Architecture of embedded Systems-Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools. ARM Architecture Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.

MODULE II

Overview of Cortex-M3: Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions. Cortex-M3 Implementation Overview: Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.

MODULE III

Cortex-M3/M4 Programming: Cortex-M3/M4 Programming: Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. Exception Programming: Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. Memory Protection Unit and other Cortex-M3 features: MPU Registers, Setting up the MPU, Power Management, Multiprocessor Communication.

MODULE IV

Cortex- M3/M4 Microcontroller: STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control.STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART.

MODULE V

Serial Bus Communication protocols: I^2C, CAN, USB, Fire wire-IEEE 1394 Bus standard, advanced serial high speed buses. Parallel Bus device protocols: ISA, PCI, PCI-X , ARM Bus, Advanced parallel high speed buses. Internet Enabled Systems-Network protocols: HTTP, TCP/IP, Ethernet.

Suggested Reading:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex –M3", 2/e, & Elsevier Inc., 2010.
2. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide- Designing and Optimizing System Software", 2006, Elsevier.
3. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual 5 /97.
4. Rajkamal, "Embedded Systems-Architecture, Programming and Design " , 2/10 TMH, 2012.
5. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education.

Course Code	Course Title						Core/ Elective
P21PC002EC	Digital IC Design						Program Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	3	-	-	-	30	70	3

Course Objectives:

1. Discuss the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay.
2. Design the Combinational Logic in CMOS.
3. Design the sequential circuit and measure the performance parameters.
4. Describe the design of arithmetic building blocks.
5. Describe the semiconductor memory design.

Course Outcomes

After completing this course, the student will be able to:

1. Appreciate the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay.
2. Understand path optimization of CMOS gates with Logical Effort.
3. Compute delay and power dissipation in both dynamic and static CMOS designs, and apply pipelining techniques to optimize Sequential Circuits.
4. Apply power reduction techniques for design of simple data path for a processor.
5. Understand the design of a 6T SRAM cell and organize a memory bank.

MODULE I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, MOSFET secondary effects, Simple Interconnect Wire models, Design rules, Sub-threshold Conduction. CMOS Inverter – Static and Dynamic Behavior, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

MODULE II

Designing Combinational Logic in CMOS: Static CMOS design: Complimentary CMOS, Rationed Logic, Pass Transistor Logic, Transmission Gate Logic, Optimizing Paths with Logical effort. **Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic, Signal Integrity Issues, Cascading Dynamic Gates**

MODULE III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles, Pipelining to optimize Sequential Circuits, Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic effects, Advanced Interconnect Techniques, Power Grid and Clock design: Power Distribution Design, Clocking and Timing Issues, Phase-Locked Loops / Delay Locked Loops.

MODULE IV

Designing Arithmetic Building Blocks: Data paths in Digital Processor Architectures, The Adder, The Multiplier, The Shifter and The Comparator. Power and Speed Trade-offs in Data path Operators: Design- Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues.

MODULE V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, SRAM Cell Layout.

Suggestive Reading:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in DSM Technology", 3rd Edition, Tata McGraw Hill, 2008
3. Wayne Wolf, Modern VLSI Design, 3rd edition, Pearson Education, 1997.
4. Neil H E Weste Kamran Eshraghian, Principles of CMOS VLSI Design a system perspective, 3rd edition, Pearson, 2005.
5. K. Eshraghian, A. Pucknell, Essentials of VLSI Circuits and Systems, PHI, 2005.

Course Code	Course Title						Core/ Elective
P21PE001EC	Software for Embedded Systems						Program Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Embedded Systems	3	-	-	-	30	70	3

Course Objectives:

1. Describe the role of Embedded Program.
2. Discuss the overview of Embedded C.
3. Analyze the Embedded Software Development Process.
4. Illustrate the object state behavior using Unified Modeling Language.
5. Discuss the web architectural frame work for Embedded System.

Course Outcomes:

After completing this course, the student will be able to:

1. Understand the role of Embedded Program.
2. Analyze the insight into overview of Embedded C.
3. Learn about Software Development Process.
4. Understand about the program modeling using UML.
5. Analyze about web architectural frame work for Embedded System.

MODULE I

Programming Embedded Systems: Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Types of memory – Memory testing – Flash Memory.

MODULE II

C and Assembly: Overview of Embedded C - Compilers and Optimization - Programming and Assembly Register usage conventions – typical use of addressing options – instruction sequencing– Procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables

MODULE III

Embedded Program and Software Development Process: Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ Inline Functions and Inline Assembly -Portability Issues - Embedded Java- Software Development process: Analysis – Design- Implementation – Testing – Validation- Debugging - Software maintenance

MODULE IV

Unified Modeling Language: Object State Behavior – UML State charts – Role of Scenarios in the Definition of Behavior Timing Diagrams – Sequence Diagrams – Event Hierarchies – Types and Strategies of Operations Architectural Design in UML Concurrency Design – Representing Tasks – System Task Diagram – Concurrent State Diagrams – Threads. Mechanistic Design – Simple Patterns.

MODULE V

Web Architectural Framework For Embedded System: Basics – Client/Server model- Domain Names and IP address – Internet Infrastructure and Routing – URL – TCP/IP protocols - Embedded as Web Client - Embedded Web servers – HTML Web security - Case study: Web-based Home Automation system.

Suggestive Reading:

1. David E.Simon: "An Embedded Software Primer", Pearson Education, 2004.
2. Michael Barr, "Programming Embedded Systems in C and C++", Oreilly, 2003.
3. H.M. Deitel , P.J. Deitel, A.B. Golldberg " Internet and World Wide Web – How to Program" Third Edition, Pearson Education, 2001. This edition is out of unit a none of its contents are referred in the syllabus.
4. Bruce Powel Douglas, "Real-Time UML, Developing Efficient Object for Embedded Systems, 2nd edition ,1999, Addison-Wesley
5. Daniel W. lewis, "Fundamentals of Embedded Software where C and Assembly meet" PHI 2002.
6. Raj Kamal, "Embedded Systems- Architecture,Programming and Design" 2 / e , TMH,2012.

Course Code	Course Title						Core/Elective
P21PE002EC	Hardware Software Co-Design						Program Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Embedded System Design	3		-	-	30	70	3

Course Objectives:

1. Describe the various Co-Design issues and Co-Synthesis algorithms.
2. Discuss about the emulation techniques and its target architecture.
3. Illustrate about the knowledge of firmware development process and tools.
4. Apply the validation methods and adaptability.
5. Apply the operation System level specification and Design

Course Outcomes:

After completing this course, the student will be able to:

1. Acquire the knowledge on various co-design models
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools.
4. Understand validation methods and adaptability.
5. Comprehend the System level specification and Design.

MODULE I

Co- Design Issues and Co- Synthesis Algorithms: Co- Design Models, Architectures, and Languages, A Generic Co-design Methodology.: Hardware software synthesis algorithms: hardware/ software partitioning, Distributed system co-synthesis.

MODULE II

Prototyping and Emulation: Prototyping and Emulation techniques, Prototyping and emulation environments, Future developments in emulation and prototyping architecture specialization techniques, System communication infrastructure. Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

MODULE III

Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

MODULE IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, Design verification, implementation verification, verification tools, interface verification

MODULE V Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Suggestive Reading:

1. Jorgen Staunstrup, Wayne Wolf, Hardware / Software Co- Design Principles and Practice, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, 2002, Hardware / Software Co- Design, Kluwer Academic Publishers.
3. Patrick R. Schaumont, Practical Introduction to Hardware/Software Co-design, 2010, Springer.

Course Code	Course Title						Core/ Elective
P21PE003EC	Reconfigurable Computing System						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
		-	-	-	30	70	3

Course Objectives

1. Discuss Application Specific IC (ASIC) fundamentals.
2. Describe various FPGA architechtures.
3. Calculate power consumption of ASIC.
4. Illustrate Interconnection, Placement and Routing schemes.
5. Apply verification and testing schemes.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the design flow of ASICs and identify the implementation tools required for simulation and synthesis of FPGA Design
2. Compare the architectural features of various FPGAs.
3. Analyze the physical design of FPGAs and CAD tools for low level design entry.
4. Estimate the placement & routing algorithms.
5. Validate the digital design and discuss the general design issues.

MODULE I

Introduction to ASIC's: Types of ASIC's, ASIC design flow, Economies of ASIC's, Programmable ASIC's: CPLD and FPGA. Commercially available CPLD's and FPGA's: XILINX, ALTERA, ACTEL. FPGA Design cycle, Implementation tools: Simulation and synthesis, Programming technologies. Applications of FPGAs

MODULE II

FPGA Logic Cell for XILINX, ALTERA and ACTEL ACT: Technology trends, Programmable I/O blocks, FPGA interconnect: Routing resources, Elmore's constant, RC delay and parasitic capacitance, FPGA design flow, Dedicated Specialized components of FPGAs

MODULE III

FPGA Physical Design: CAD tools, Power dissipation, FPGA Partitioning, Partitioning methods. Floor planning: Goals and objectives, I/O, Power and clock planning, Low-level design entry.

MODULE IV

Placement: Goals and objectives, Placement algorithms: Min-cut based placement, Iterative Improvement and simulated annealing. Routing, introduction, Global routing: Goals and objectives, Global routing methods, Back-annotation. Detailed Routing: Goals and objectives, Channel density, Segmented channel routing, Maze routing, Clock and power routing, Circuit extraction and DRC.

MODULE V

Verification and Testing: Verification: Logic simulation, Design validation, Timing verification. Testing concepts: Failures, Mechanism and faults, Fault coverage. Design Applications: General Design issues, Counter Examples, A Fast DMA controller, Designing adders and accumulators with Xilinx Architecture.

Suggested Reading:

1. Michael John Sebastian Smith, Application Specific Integrated Circuits, Pearson Education Asia, 3rd edition 2001.
2. Pak and Chan, Samiha Mourad, Digital Design using Field Programmable Gate Arrays, Pearson Education, 1st edition, 2009.
3. S.Trimberger,Edr, Field Programmable Gate Array Technology,Kluwer Academic Pub,1994.

Course Code	Course Title						Core/Elective
P21PE004EC	Advanced Computer Architecture						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Computer Organization and Architecture	3	-	-	-	30	70	3

Course Objectives

1. Discuss fundamentals of computer design.
2. Analyze quantitatively the performance parameters for different architectures.
3. Explain Instruction Level Parallelism and its limitations.
4. Illustrate multi-processors and thread level parallelism.
5. Describe Interconnection networks.

Course Outcomes

After completing this course, the student will be able to:

1. Comprehend the organization of the CPU and data path design.
2. Compare the concepts of Hardwired and Micro programmed Control Unit design of general purpose computer.
3. Understand the memory organization and hierarchy.
4. Analyze I/O Interfacing concepts.
5. Understand the Interconnection networks.

MODULE I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, operations in the instruction set. Data path Design : Case studies-DMA controller

MODULE II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory. Describe RISC architecture, memory hiravachy and issues the pipelining architecture

MODULE III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

MODULE IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

MODULE V

Inter Connection Networks: Introduction: Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

Suggested Reading:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.
2. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw Hill.
3. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", McGraw Hill.
4. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture – A Design Space Approach", Pearson Education.

Course Code	Course Title						Core/Elective
P21PE005EC	Low Power VLSI Design						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design		-	-	-	30	70	3

Course Objectives:

1. Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
2. Characterize and model power consumption & understand the basic analysis methods.
3. Discuss leakage sources and power reduction techniques.
4. Describe power estimation techniques and power minimization techniques.
5. Design basic low power memory circuits.

Course Outcomes:

After completing this course, the student will be able to:

1. Analyze the basic concepts of sources of power dissipation in digital IC systems and impact of power on system performance and reliability.
2. Understand model power consumption and basic analysis methods.
3. Explore the leakage sources and power reduction techniques.
4. Analyze the different power estimation and power minimization techniques.
5. Develop low power memory circuits.

MODULE I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{dd} & V_t on speed, constraints on V_t reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

MODULE II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

MODULE III

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew V_s. Tolerable skew, chip & package co- design of clock network.

MODULE IV

Logic Synthesis for Low Power: Power Estimation Techniques, Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

MODULE V

Low Power Memory Design: Sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM, low power DRAM circuits, low power SRAM circuits.

Suggested Reading:

1. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
2. A.P. Chandrasekaran and R.W. Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
4. J.B. Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

Course Code	Course Title						Core/Elective
P21PE006EC	Semiconductor Device Modeling						Program Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Semiconductor Physics, Linear Integrated Circuits	3	-	-	-	30	70	3

Course Objectives:

1. Describe the characteristics and modeling of Diode.
2. Discuss about the BJT model parameters and conventions.
3. Illustrate about the JFET model parameters and conventions.
4. Explain the levels, models and structures of the Metal Oxide Semiconductor Transistor.
5. Analyze BJT, Metal Oxide Semiconductor Transistor parameter measurements.

Course Outcomes:

After completing this course, the student will be able to:

1. Understand the basics characteristics and modeling of Diode.
2. Analyze BJT model parameters and conventions.
3. Develop Comprehensive idea on JFET model parameters and conventions.
4. Understand the levels, models and structures of the Metal Oxide Semiconductor Transistor.
5. Explore the BJT, Metal Oxide Semiconductor transistor parameter measurements.

MODULE I

PN-Junction Diode and Schottky Diode:

DC Current Voltage Characteristics, Static Model, Large Signal Model, Small Signal Model, Schottky Diode and its implementation in SPICE 2, Temperature and Area effects on the Diode Model Parameter SPICE 3 Models PSPICE Models.

MODULE II

Bipolar Junction Transistor (BJT):

Transistor Conventions and Symbols, Ebers –Moll Static Model, Ebers- Moll Large Signal Model, Ebers-Moll Small Signal Model, Gummel- Poon Static Model, Gummel-Poon Large Signal Model, Gummel- Poon Small Signal Model, Temperature and Area Effects on the BJT Model Parameters, Power BJT model, SPICE 3 Models, PSPICE Models.

MODULE III

Junction Field-Effect Transistor (JFET):

Static Model, Large Signal Model and its implementation in SPICE 2, Small Signal Model and its implementation in SPICE 2, Temperature and Area Effects on the JFET Model Parameters, SPICE 3 Models, PSPICE Models.

MODULE IV

Metal –Oxide Semiconductor Transistor (MOST):

Structure and Operating Regions of the Metal Oxide Semiconductor Transistor, Level, Static Model, Level 2 Static Model, Level 1 and Level 2 Large Signal Model, Level 3 Static Model, Level 3 Large Signal Model, Effect of Series Resistances, effect of temperature on the Metal Oxide Semiconductor Transistor model parameters, SPICE 3 Models, PSPICE Model.

MODULE V

BJT, Metal Oxide Semiconductor Transistor Parameter Measurements:

Input and Model parameters, Parameter Measurements, Level 1 Model Parameters, Level 2 Model (Long-Channel) parameters, Level 2 Model (Short-Channel) parameters, Level3 Model Parameters, Measurements of capacitance, Noise, Distortion.

Suggestive Reading:

1. Giuseppe Massobrio & Paolo Antognetti, "Semiconductor Device Modeling with Spice", second edition, Tata McGraw – Hill
2. Semiconductor Devices, Physics and Technology, Simon Sze, Ming- Kwe Lee, 3ed, ISV, WILEY Student Edition
3. Semiconductor Device Modelling, Snowden, Springer Publication

Course Code	Course Title						Core/Elective
P21PE007EC	System on Chip Design						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	30	70	3

Course Objectives

1. Illustrate Integration of hardware and software on a chip.
2. Describe various processors.
3. Design of Memory for system on chip.
4. Discuss with Interconnection of various devices and reconfiguration.
5. Explore various application of system on chip.

Course Outcomes

After completing this course, the student will be able to:

1. Apply fundamental knowledge of digital logic design to modeling and analysis of low power in processor design.
2. Understand the design concepts of processor, pipelining concepts, ARM Development Tools and Interfacing ARM with Co-processors.
3. Analyze the concepts of Memory Hierarchy, Cache design and Memory Management.
4. Contrast various interconnect schemes for system Development.
5. Develop a simple SoC for re-configurability/low power/ASIP/NISC etc.

MODULE I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing, System level interconnection, an approach for SOC Design, System Architecture and Complexity.

MODULE II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

MODULE III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

MODULE IV

Architectural Support for System Development – ARM: The ARM Memory Interface, AMBA, ARM reference peripheral specification, Hardware system prototyping tools, The ARMUlator, JTAG Boundary scan test architecture, The ARM Debug architecture, Embedded Trace, Signal processing support.

MODULE V

Application Studies / Case Studies: SOC Design approach, AES algorithms - Design and evaluation, Image compression – JPEG compression.

Suggested Reading:

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiley India Pvt. Ltd
2. Steve Furber, ARM System on Chip Architecture, 2nd Ed., Addison Wesley Professional,2000.
3. Ricardo Reis, "Design of System on a Chip: Devices and Components, 1st Ed., Springer,2004.
4. Jason Andrews, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Newnes, BK and CDROM.
5. Prakash Rashinkar, Peter Paerson and Leena Singh L, System on Chip Verification – Methodologies and Techniques, Kluwer Academic Publishers,2001.

Course Code	Course Title						Core/Elective
P21PE008EC	VLSI for Signal Processing						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Digital Signal Processing	3	-	-	-	30	70	3

Course Objectives:

1. Explain the Pipelining and Parallel processing concepts for Digital Signal Processors.
2. Analyze the Unfolding algorithm, Folding transformation and Systolic array design.
3. Describe the Algorithmic Strength Reduction in FIR filters, Pipelining and Parallel processing for IIR filters.
4. Analyze the Bit level Arithmetic Architectures like carry-ripple and carry-save array multipliers.
5. Discuss the operation of Numerical Strength Reduction through synchronous and asynchronous pipelining.

Course Outcomes:

After completing this course, the student will be able to:

1. Analyze the Pipelining and Parallel processing concepts for Digital Signal Processors.
2. Develop the Unfolding algorithm, folding transformation and Systolic array design.
3. Analyze the Algorithmic Strength Reduction in FIR filters, Pipelining and parallel processing for IIR filters.
4. Analyze the Bit level Arithmetic Architectures like carry-ripple and carry-save array multipliers.
5. Understand the operation of Numerical Strength Reduction through synchronous and asynchronous pipelining.

MODULE I

Digital Signal Processing Systems: Introduction to DSP Processors and Systems- Typical DSP algorithms, Data flow graph representations, Loop bound and iteration bound, Longest Path Matrix algorithm, Pipelining and Parallel processing - Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power, Retiming - definitions and properties, Retiming techniques.

MODULE II

Unfolding, Folding And Systolic Architectures: Unfolding Algorithm- Properties and Applications of Unfolding, Folding Transformation, Systolic Array design- FIR systolic arrays, Selection of Scheduling Vectors, Matrix multiplication and 2D systolic array design.

MODULE III

Fast Convolution And Algorithmic Strength Reduction: Cook-Toom Algorithm, Inefficient/Efficient Single Channel Interleaving, Cyclic convolution, Algorithmic strength reduction in FIR filters and DCT, Look-Ahead pipelining in first-order IIR filters, Parallel processing of IIR filters ,Combined pipelining and parallel processing for IIR filters, Pipelined adaptive digital filters.

MODULE IV

Bitlevel Arihtmetic Architectures: Scaling and Round-off Noise- Computation, Round-off Noise in Pipelined first-order IIR Filters, BitLevel Arithmetic Architectures: Parallel Multipliers with sign extension, Parallel Carry-Ripple Array Multipliers, Parallel Carry-Save Array Multiplier, 4x4 bit Baugh-Wooley Carry-Save Multiplier, Bit-Serial FIR Filter Design and Implementation.

MODULE V

Numerical Strength Reduction: Numerical Strength Reduction, Sub expression Elimination, Multiple Constant Multiplication, Iterative Matching, Linear Transformations, Synchronous, Wave and Asynchronous Pipelining, Synchronous Pipelining and Clocking Styles, Clock Skew and Clock Distribution in bit-level Pipelined VLSI Designs, Wave Pipelining, Asynchronous Pipelining.

Suggested Reading:

1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 1999.
2. U.Meyer Baese , "Digital Signal Processing with Field Programmable Arrays", Springer, 2007.
3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog, Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

Course Code	Course Title						Core/Elective
P21MC001CS	**Research Methodology and IPR**						**Mandatory Course**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

To make students to

1. Motivate to choose research as career
2. Formulate the research problem, prepare the research design
3. Identify various sources for literature review and data collection report writing
4. Equip with good methods to analyse the collected data
5. Know about IPR copyrights

Course Outcomes

At the end of this course, students will be able to**:**

1. Define research problem, review and asses the quality of literature from varioussources
2. Improve the style and format of writing a report for technical paper/ Journal report, understand anddevelop various research designs
3. Collect the data by various methods: observation, interview, questionnaires
4. Analyse problem by statistical techniques: ANOVA, F-test, Chi-square
5. Understand apply for patent and copyrights

MODULE - I

Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods Verses Methodology, Research Process, Criteria of GoodResearch, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem

MODULE - II

Literature Survey and Report writing: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Need of Review, Guidelines for Review, Recordof Research Review.

Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanism of writing a report. **Research Proposal Preparation**: Writing a Research Proposal and Research Report, Writing Research Grant Proposal.

MODULE - III

Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Steps in sample design, types of sample designs.

MODULE - IV

Data Collection and Analysis: Methods of data collection, Data organization, Methods of data grouping, Diagrammatic representation of data, Graphic representation of data. Importance of Parametric, non- parametric test, testing of variance of two normal populations, use of Chi-square, ANOVA, F-test, z-test

MODULE - V

Intellectual Property Rights: Meaning, Nature, Classification and protection of Intellectual Property, The main forms of Intellectual Property, Concept of Patent, Patent document, Invention protection, Granting ofpatent, Rights of a patent, Licensing, Transfer of technology.

Suggested Readings:

1. C.R Kothari, Research Methodology, Methods & Technique ; New Age International Publishers,2004
2. R. Ganesan, Research Methodology for Engineers, MJP Publishers, 2011
3. Y.P. Agarwal, Statistical Methods: Concepts, Application and Computation, Sterling Publications Pvt. Ltd., New Delhi, 2004
4. G.B. Reddy, Intellectual Property Rights and the Law 5th Ed. 2005 Gogia Law Agency
5. Ajit Parulekar and Sarita D'Souza, Indian Patents Law – Legal & Business Implications, MacmillanIndia Ltd, 2006

Course Code	Course Title						Core / Elective
P21AD001HS	English for Academic and Research Writing						Humanities and Social Sciences
Prerequisite	Contact Hours per Week				CIE	SEE	Core
	L	T	D	P			Credits
NIL	2				30	70	0 (audit course)

Course Objectives:

1. To learn the Features of Academic Writing
2. To write Essays, Reports, Reviews, Abstracts and Proposals
3. To demonstrate Academic Writing Skills
4. To analyse the Research Process
5. To apply appropriate structure to a Research Document

Course Outcomes: At the end of the course, the student should be able to

1. learn the Features, Tone, Style, and Ethics pertaining to Academic Writing
2. write Essays, Reports, Reviews, Abstracts and Proposals
3. demonstrate Academic Writing Skills such as Paraphrasing, Summarizing, Quoting, Rewriting and Expansion
4. analyse the Research Process from Selection of Topic, Formulation of Hypothesis, Collection, Analysis, Interpretation and Presentation of Data
5. apply appropriate structure to a Research Document,such as selection of Title, writing the Abstract, Introduction, Literature Survey, Methodology, Discussion, Findings/Results, Conclusion and citing Document Sources (IEEE style)

MODULE I

Features of Academic Writing Language: Clear, Correct, Concise, Inclusive; **Tone**: Formal, Objective, Cautious;
Style: Appropriate, Accurate, Organized; **Ethics**: Honesty, Integrity, Responsibility, Accountability

MODULE II

Kinds of Academic Writing : Essays, Reports, Reviews, Abstracts, Proposals

MODULE III

Academic Writing Skills : Paraphrasing; Summarizing; Quoting; Rewriting; Expansion

MODULE IV

Research Process : Selection of Topic, Formulation of Hypothesis, Collection of Data, Analysis of Data, Interpretation of Data, Presentation of Data

MODULE V

Structure of a Research Document: Title, Abstract, Introduction, Literature Survey, Methodology, Discussion, Findings/Results, Conclusion, Documenting Sources (IEEE style)

Suggested Reading :

1. Bailey, S. (2014). Academic writing: A handbook for international students. Routledge.
2. Gillett, A., Hammond, A., &Martala, M. (2009). Inside track: Successful academic writing. Essex: Pearson Education Limited.
3. Griffin, G. (2006). Research methods for English studies. Edinburgh: Edinburgh University Press.
4. Silyn-Roberts, Heather. (2013). Writing for Science and Engineering: Papers, Presentations and Reports(2nd ed.). Elsevier.
5. Lipson, Charles (2011). Cite right: A quick guide to citation styles; MLA,APA, Chicago, the sciences, professions, and more (2nd ed.). Chicago[u.a.]: University of Chicago Press.

Course Code	Course Title						Core/ Elective
P21PC801EC	EMBEDDED SYSTEM DESIGN LAB						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	2	50	-	1

Course Objectives

1. Describe the IDE tool for developing and executing the programs using ARM Cortex M3 (LPC 1768).
2. Illustrate the usage of on-chip PWM for DC motor control.
3. Explain programming with Cortex-M3/M4 to interface devices like Stepper Motor for controlling the direction.
4. Illustrate the interfacing of Cortex-M3 Microcontroller with DAC, LCD, and LED to develop real time projects.
5. Discuss the interface devices like Relay and Buzzer to ARM microcontroller and analyze the working of GPIO, on-chip peripherals of ARM.

Course Outcomes

After completing this course, the student will be able to:

1. Use the IDE tool effectively for developing and executing the programs using ARM Cortex M3 (LPC 1768).
2. Comprehend the usage of on-chip PWM for DC motor control.
3. Interface devices like Stepper Motor to control the direction.
4. Interface devices like DAC, LCD, and LED to develop real time projects.
5. Develop the logic to interface devices like Relay and Buzzer to ARM microcontroller and analyze the working of GPIO, on-chip peripherals of ARM.

Programming in ARM Cortex M3 (LPC 1768)

1. UART0 test Demonstration (To display HELLO WORLD)
2. DC motor control using on chip PWM
3. Stepper motor Direction control
4. LCD Interfacing
5. Program to generate Triangular, square and sinusoidal wave with DAC.
6. Toggle of LEDs using external interrupts.
7. Seven segment display
8. Relay/buzzer/Led test

Course Code	Course Title						Core/Elective
P21PC802EC	Digital IC Design Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	2	50	-	1

Course Objectives:

1. Design combinational and sequential circuits using Verilog HDL.
2. Apply simulation tool for combinational and sequential circuits RTL code and synthesize using EDA tools.
3. Apply Floor plan for designed schematic of the various logic circuits using EDA tool.
4. Apply placement algorithms for the various logic circuits using EDA tool.
5. Apply routing algorithms for the various logic circuits using EDA tools.

Course Outcomes:

After completing this course, the student will be able to:

1. Develop combinational and sequential circuits using Verilog HDL.
2. Analyze the output of simulation results for combinational and sequential circuits RTL code and synthesize using EDA tools.
3. Analyze Floor plan for designed schematic of the various logic circuits using EDA tool.
4. Evaluate placement algorithms for the various logic circuits using EDA tool.
5. Analyze routing algorithms for the various logic circuits using EDA tools.

PART – A

Design, simulation and synthesis of

1. Adder and Subtractor
2. Multiplexer and Demultiplexer
3. Encoder and Decoder
4. ROM array
5. Up/Down Counter
6. Finite State Machine

PART - B

Floor plan, Placement and Routing of

1. Adder and Subtractor
2. Multiplexer and Demultiplexer
3. Encoder and Decoder
4. ROM array
5. Up/Down Counter
6. Finite State Machine

NOTE: At least 10 experiments are to be performed.

Course Code	Course Title						Core/ Elective
P21PC003EC	Real Time Operating Systems for Embedded System						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	1	-	-	30	70	4

Course Objectives

1. Describe the structure of Operating System.
2. Distinguish between Hard and Soft Real Time Systems and analyze real time scheduling algorithms
3. Illustrate the concept of Real Time Kernel and implementation of Inter Process Communication.
4. Discuss the features of Vx Works and compare the commercially available RTOS's.
5. Describe the features of UNIX operating system and differentiate between UNIX and POSIX.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the fundamental structure of Operating System.
2. Compare between Hard and Soft Real time systems and analyze real time scheduling algorithms.
3. Analyze the concept of Real Time Kernel and implementation of Inter Process Communication.
4. Analyze the features of VxWorks and compare the commercially available RTOS's.
5. Explore the features of UNIX operating system and differentiate between UNIX and POSIX.

MODULE I

Fundamentals of Operating System: Structures of Operating System: Monolithic, Microkernel, Layered, Exo-kernel and Hybrid kernel structures, Operating System objectives and functions, Virtual Computers, Interaction of Operating system and Hardware architecture.

Evolution of operating systems: Batch, Multi programming, Multitasking, Multiuser, Parallel, Distributed and Real-Time Operating System.

MODULE II

Real Time Operating System: Hard versus Soft Real-time systems, Jobs & Processors, Release Times, Deadlines and timing constraints, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems. **Real Time Scheduling Algorithms**: Weighted Round Robin Approach, Priority Driven Approach, EDF scheduling Algorithm, Rate Monotonic Scheduling. Challenges in validating timing constraints in priority driven systems.

MODULE III

Real Time Kernel: Differences between Traditional OS and RTOS, Real-time System Concepts. RTOS Kernel & Issues in Multitasking: Task Assignment, Task Priorities, Inter Task Communication & classical problems of Synchronization, Definition of Context Switching, ISRs. Critical Section. Inter Process Communication (IPC): IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

MODULE IV

Elementary Concepts of Vx Works: Multitasking and Task State Transition: Task Control, Task Creation and Activation, Task Stack, Task Names and IDs, Task Options, Task Information, Task Deletion and Deletion Safety.

Memory Management: Virtual to Physical Address Mapping. Comparison of RTOS and VxWorks, µC/OS-II and RT Linux for Embedded Applications.

MODULE V

Brief Review of Unix Operating Systems: UNIX Kernel: File system, Concepts of Process, Concurrent Execution & Interrupts. Process Management: forks and execution, Programming with system calls, Process Scheduling. Shell programming and filters.

Portable Operating System Interface (POSIX): IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability.

Suggested Reading:

1. Jane W.S. Liu," Real Time Systems, Pearson Education", Asia, 2001.
2. K.C. Wang, "Embedded and Real Time Operating Systems", Springer International Publishing
3. Betcnhof, D.R., "Programming with POSIX threads", Addison - Wesley Longman, 1997.
4. Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.
5. Jean.J. Labrosse, "MicroC/OS-II", The CMP Books.
6. C.M. Krishna and G. Shin, Real Time Systems, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

Course Code	Course Title						Core/ Elective
P21PC004EC	Analog and Mixed Signal IC Design						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Digital IC Design		-	-	-			4

Course Objectives

1. Describe the concepts of advanced current mirrors and band-gap reference circuits.
2. Discuss the applications of OP Amp: comparator and oscillator.
3. Explain the switched capacitor based circuits.
4. Distinguish between the features of mixed signal circuits and other circuits.
5. Analyze mixed signal circuits like switched capacitor circuits, data converters etc., starting from fundamentals.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the basic concepts of CMOS circuits, analyze and design current sources/sinks/mirrors
2. Understand the concepts of OPAMPs and its characteristics and analyze the operation of comparators and various oscillators.
3. Explore the concepts of switched capacitor circuits
4. Comprehend the features of sample and hold circuits and apply them to design Nyquist rate data converter circuits.
5. Analyze and design oversampling rate data converter circuits.

MODULE I

Small Signal Model and Current Mirrors: Brief review of Small Signal and Large Signal Model of BJTs and MOSFETs, Current Mirrors and Single Stage Amplifiers – Simple CMOS current mirror, common source amplifier, source follower, common gate amplifier, cascode amplifiers. Source degenerated current mirrors. High out impedance – current mirrors, cascode gain stage Wilson current mirror, MOS differential pair and gain stage. Differential pairs with current mirror loads MOS and bipolar widlar current sources, Band gap reference circuits.

MODULE II

Operational Amplifiers: Basic two stage MOS Operational amplifier–Characteristic parameters, two stage MOS Op-Amp with Cascodes. MOS Telescopic-cascode Op- Amp. MOS Folded cascode op-amp. MOS Active Cascode Op-Amp. Fully differential folded cascode op-amp. Current feedback op-amps. Stability and frequency compensation of op- amps. Phase margin in op-amps.

MODULE III

Comparators: Op-Amp Based Comparators, Charge Injection Errors – Latched Comparators – CMOS and BiCMOS Comparators .Switched capacitor circuits: Basic building blocks; basic operation and analysis, inverting and non-inverting integrators, signal flow diagrams, first order filter.Sample and hold circuits - Performance requirements, MOS sample and hold basics, clock feed through problems,

MODULE IV

Data Converters-I: S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations. Data converter fundamentals - performance characteristics, ideal D/A and A/D converters, quantization noise. Nyquist rate D/A converters – decoder based converter, binary-scaled converters. Thermometer code converters, current mode converters.

MODULE V

Data Converters-II: Nyquist rate A/D Converters: Integrated converters – successive approximation converters, cyclic A/D converters, Flash or parallel converters, Two step A/D converters, pipelined A/D converters. Over sampling converters. Over sampling without noise shaping over sampling and with noise shaping, system architecture – digital decimation filters.

Suggested Reading:

1. Paul. R. Gray & Robert G. Major, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill. 2002
4. Jacob Baker. R. et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.
5. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.

Course Code	Course Title						Core/Elective
P21PE009EC	Internet of Things						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	3	1	-	-	30	70	3

Course Objectives:

1. Discuss the fundamentals of IoT and its applications and requisite infrastructure.
2. Describe Internet principles and communication technologies relevant to IoT.
3. Discuss hardware and software aspects of designing an IoT system.
4. Describe concepts of cloud computing and Data Analytics.
5. Explain IoT applications

Course Outcomes:

1. Analyze fundamentals of IoT and its applications.
2. Apply Internet principles and communication technologies relevant for IoT.
3. Develop API and its embedded programming.
4. Develop software and hardware aspects of an IoT system.
5. Explore IoT applications in various fields of engineering.

MODULE I

Introduction to Internet of Things: Definition and Characteristics of IoT, Physical Design of IoT: Things in IoT, IoT protocols, Logical Design of IoT: IoT functional Blocks, Communication Models, APIs, IoT enabling Technologies: Wireless Sensor Networks, Cloud Computing, Big Data Analytics

IoT Applications: Smart Home, Smart Cities, Smart Environment, Smart Energy, Smart Retail and Logistics, Smart Agriculture and Industry, Smart Industry and smart Health

MODULE II

Internet Principles and communication technology: Internet Communications: An Overview – IP, TCP, IP protocol Suite, UDP. IP addresses – DNS, Static and Dynamic IP addresses, MAC Addresses, TCP and UDP Ports.

Application Layer Protocols: HTTP, HTTPS, Cost Vs Ease of Production, Prototypes and Production, Open Source Vs Closed Source.

Prototyping Embedded Devices: Sensors, Actuators, Microcontrollers, SoC, Choosing a platform.

Prototyping Hardware platforms: Arduino, Raspberry Pi. Prototyping the physical design – Laser Cutting, 3D printing, CNC Milling

MODULE III

API Development and Embedded programming: Getting started with API, writing a new API, Real time Reactions, Other Protocols, Techniques for writing embedded code, Memory management, Performance and Battery Life, Libraries, Debugging.

Developing Internet of Things: IoT design Methodology, Case study on IoT System for weather monitoring.

MODULE IV

IoT Systems - Logical Design using Python : Introduction to Python, Data Types and Structures, Control Flow, Functions, Modules, Packages, File Handling, Date/Time Operations., Classes, Python packages for IoT

IoT Physical Devices and Endpoints: Raspberry Pi, Interfaces of Pi, Programming pi with Python - Controlling LED and LDR using Pi with python programming.

MODULE V

Cloud computing and Data analytics and IoT Product Manufacturing: Introduction to Cloud storage models and Communication APIs, Amazon web services for IoT, Skynet IoT Messaging Platform. Introduction to Data Analytics for IoT . Case studies illustrating IoT Design – Smart Lighting, Weather Monitoring, Smart Irrigation. Business model for IoT product manufacturing, IoT Start-ups, Mass manufacturing, Ethical issues in IoT.

Suggested Readings:

1. Vijay Madisetti, Arshdeep Bahga, Internet of Things (A Hands-On-Approach), VPT Publisher, 1st Edition, 2014.
2. Adrian McEwen (Author), Hakim Cassimally, Designing the Internet of Things, Wiley India Publishers.
3. Kenneth A Lambert and B.L. Juneja, Fundamentals of Python, Cengage Learning.
4. O.Vermesan, P Friess Internet of Things - Converging Technologies for Smart Environments and Integrated Ecosystems, River Publishers, 2013.
5. Arshdeep Bahga, Internet of things -A hands on Approach, Universities press.

Course Code	Course Title						Core/ Elective
P21PE010EC	Network Embedded Applications						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Computer Networks	3	-	-	-	30	70	3

Course Objectives

1. Explain the concept of embedded networking and communication requirements for Embedded Networking.
2. Describe the fundamentals of CAN open and analyze the data handling for communication between CAN open devices.
3. Comprehend the network programming framework and analyze the CAN open Manager.
4. Discuss system requirements for configuring networks in CAN open framework.
5. Describe key features for implementing the CAN Technology.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the concept of embedded networking and communication requirements for Embedded Networking.
2. Explore the fundamentals of CAN open and analyze the data handling for communication between CAN open devices.
3. Comprehend the network programming framework and analyze the CAN open Manager.
4. Identify system requirements for configuring networks in CAN open framework.
5. Analyze key features for implementing the CAN Technology.

MODULE I

Understanding Embedded Networking:

Embedded Networking, Code requirements for Embedded System, Communication Requirements for Embedded Networking, the domain of Embedded networking, Constraints imposed by Host, Constraints imposed by the application, Distributed Synchronization.

MODULE II

Introduction to CAN open: From application level, Using identifiers & objects, CAN open Object dictionary, EDS, DCI, Accessing CAN open Object Dictionary, Handling Process Data, Network Management.

MODULE III

CAN open: Frameworks & Profiles overview, CAN Open standard documents, The NMT Master, Application- Supporting functionalities in CAN open, The SDD Manager & Dynamic SDD Connections, The Configuration Manager, The CAN open Manager, Device Profile for encoder.

MODULE IV

Configuring CAN open: System requirements, Choosing the Devices & Tools, Configuring Single Devices, Overall Networks Configuration, Networks Simulation, Network communications, Advanced features and Testing.

MODULE V

CAN Technology: Introduction to CAN, Physical Layer, Signal States, Signal levels, Wiring, Connectors, Selecting a CAN Controller, Performance, Hardware Filtering, Different CAN implementations, Physical Interfaces, Code, Data and CPU Performance Requirements.

Suggested Reading:

1. Olaf Pfeiffer, Andrew Ayre, Chritian Keydel, Embedded Networking with Can and Canopen, Copperhill Media, 2008.
2. Wolfhard Lawrenz, CAN System Engineering: From Theory to Practical Applications, Springer Science & Business Media, 2013.
3. Wilfried Voss , A Comprehensible Guide to Controller Area Network, Copperhill Technologies Corporation, 2008,

Course Code	Course Title						Core/Elective
P21PE011EC	Embedded System Design Using ARM Processors						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	30	70	

Course Objectives

1. Describe the basics ARM architecture programming model, tools and its instruction set.
2. Explain the Architectural Support for High-level languages.
3. Describe the fundamentals of Thumb instruction set.
4. Discuss about ARM Processor Cores including the strong ARM.
5. Explain the basics of Embedded ARM in various Applications.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the basics of ARM architecture.
2. Analyze Architectural Support for High-level languages.
3. Analyze the fundamentals of Thumb Instruction set.
4. Understand about the ARM Processor Cores.
5. Develop the design for manufacturability and yield.

MODULE I

ARM Architecture: Acron RISC machine, architectural inheritance, ARM programmer model, ARM development tools, ARM assembly language programming ,data processing instructions, ARM inheritance set.

MODULE II

ARM Software: Architectural support for high-level languages, abstraction in software design, old types, floating point data types expressions, conditional loops, function & procedures.

MODULE III

The Thumb Instruction Set: The thumb bit in the CPSR, programming model, branch instructions, software interrupt instruction, data processing instructions, multiple register data transfer instructions, breakpoint instructions, implementation

MODULE IV

ARM Processor Cores:ARM77DMZ, ARM 8, ARM 97DMZ, ARM 740T, ARM 810, the strong ARM SA-110.

MODULE V

Embedded ARM Applications: VLSI Ruby II advanced communication processor, VLSI ISDN subscriber processor, ERRICCSON- VLSI software tools baseband controllers, AMULET asynchronous ARM processors.

Suggested Reading:

1. Steve Furber, ARM System-on-Chips Architecture.
2. ARM Assembly Steve Furber Language –CRC .
3. G. Osborn, Embedded microcontroller and processor design: (Pearson).
4. Frank Vahid, Embedded Systems, Wiley India, 2002
5. Jonathan W. Valvano, Embedded Microcomputer Systems – Real Time Interfacing, Cengage Learning; Third or later edition.

Course Code	Course Title						Core/ Elective
P21PE012EC	Distributed Embedded Computing						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	30	70	3

Course Objectives

1. To have a knowledge of the Hardware Infrastructure
2. To understand the concept of Internet
3. To have a knowledge of the using of JAVA in Distributed Embedded Computing
4. To understand embedded computing architectures

Course Outcomes

After completing this course, the student will be able to:

1. Understand of the Hardware Infrastructure
2. Understand the concept of Internet
3. Have a knowledge of the using of JAVA in Distributed Embedded Computing
4. Understand embedded computing architectures

MODULE I

The Hardware Infrastructure: Broad Band Transmission facilities, Open Interconnection standards, Local Area Networks, Wide Area Networks, Network management, Network Security, Cluster computers.

MODULE II

Internet Concepts: Capabilities and limitations of the internet, Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

MODULE III

Distributed Computing Using Java: IO streaming, Object serialization, Networking, Threading, RMI, Multicasting, Distributed Databases, Embedded Java Concepts, Case Studies**.**

MODULE IV

Embedded Agent: Introduction to the embedded agents, Embedded agent design criteria, Behaviour based, Functionality based embedded agents, Agent co-ordination mechanisms and Benchmarks Embedded-Agent. Case study: Mobile robots.

MODULE V

Embedded Computing Architecture: Synthesis of the information technologies of distributed embedded systems, Analog/Digital Co-design, Optimizing functional distribution in complex system design, Validation and fast prototyping of multiprocessor system-on-chip , A new dynamic scheduling algorithm for real-time multiprocessor systems.

Suggested Reading:

1. Dietel & Dietel, "JAVA how to program", Prentice Hall 1999.
2. Sape Mullender, "Distributed Systems", Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, "Distributed Systems – Concepts and Design", Addison –Wesley 1988.
4. Bernd Kleinjohann, "Architecture and Design of Distributed Embedded Systems", University of Paderborn/C-Lab Germany, Kluwer Academic Publishers, Boston, April 2001, 248 pp.

Course Code	Course Title						Core/Elective
P21PE013EC	System Verilog						Programme Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Digital Circuits using Verilog	3	-	-	-	30	70	3

Course Objectives

1. Explain the basics of System Verilog.
2. Describe Combinational Logic blocks using System Verilog.
3. Illustrate Sequential Logic blocks using System Verilog.
4. Analyze the ability in writing test benches for verification.
5. Discuss models using System Verilog.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the basic syntax and functions of System Verilog
2. Develop the knowledge of System Verilog in building Combinational Logic Blocks
3. Develop the knowledge of System Verilog in building Sequential Logic Blocks
4. Analyze the functionality of the design using Test Benches
5. Develop applications using the knowledge gained in System Verilog

MODULE I

Introduction: Introduction to System Verilog, System Verilog for declaration spaces – packages, compilations, unit declarations, Simulation time units and precision, literal values & built –in data types, user defined data types, Arrays, Structures and Unions.

MODULE II

Combinational Logic using System Verilog Gate Models: Modules & Files, Basic Gate Models, A simple Net List, Logic Values, Continuous Assignments, Delays, Parameters, Test Benches, Multiplexers, Decoders, Priority Encoder, Adders, Parity Checkers, Test benches.

MODULE III

Sequential Logic using System Verilog Gate Models: Latches, Flip Flops, JK and T Flip Flops, Registers, Counters, Memory, Sequential multiplier, Synchronous Sequential Systems, Models of Synchronous Sequential Machines, ASMs, Sate Machines in System Verilog.

MODULE IV

Test Benches: Basic Test Bench, Test Bench structure, Constrained Random Simulation generation, Assertion based verification, System Verilog Simulation and Synthesis

MODULE V

Verification guide lines: Introduction- Verification process, plan, Methodology. A complete design modeled with System Verilog – ATM example (other examples may also be included)

Suggestive Reading:

1. Stuart Sutherland, Simon Davidmann and Peter Flake, System Verilog for Design, Second Edition, Springer Publications.
2. Mark Zwolinski, Digital System Design with System Verilog, Prentice Hall Publications, 2009
3. Chris Spear, System Verilog for Verification, Springer Publications.

Course Code	Course Title						Core/Elective
P21PE014EC	**Multi Gate MOSFET Technology**						**Program Elective**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design		**-**	**-**	**-**	**30**	**70**	**3**

Course Objectives

1. Understand the transition from single Gate to Multi Gate technology
2. Understand the concepts of Multi Gate MOSFET's
3. Familiarize with the Physics of Multi Gate MOSFET's
4. Analyze the mobility in Multi Gate MOSFET's
5. Design circuits using Multi Gate MOSFET's

Course Outcomes

After completing this course, the student will be able to:

1. Understand the need for moving from Single Gate Technology to Multi Gate Technology
2. Analyze the concepts of Multi Gate MOSFETs
3. Develop knowledge of Physics in Multi Gate MOSFETs
4. Develop the analytical capability on concepts of Mobility
5. Develop circuits using Multi Gate MOSFET's

MODULE I

The SOI MOSFET: MOSFET scaling, Short Channel Effects, Gate Geometry and Electrostatic integrity, Single Gate SOI MOSFET, Double Gate SOI MOSFET, Triple Gate SOI MOSFET, Surrounding Gate SOI MOSFET, Multi Gate MOSFET memory devices.

MODULE II

Multi Gate MOSFET Technology: Introduction, Active area – Fins: Fin Width, Fin Height, Fin pinch, Fin crystal orientation, Fin surface preparation, Fin Bulk Silicon. Gate stack – patterning, threshold voltage, Gate work function requirements, Source / Drain Resistance and Capacitance, Mobility, contacts to the Fin,

MODULE III

Physics of Multi Gate MOS system: Device electrostatics, Double Gate MOS System – Modeling assumptions, Gate Voltage effect, Semiconductor thickness effect, Asymmetry effects, Oxide thickness effect, electron tunnel current. 2-D confinement.

MODULE IV

Mobility in Multi Gate MOSFETs: Introduction, Double Gate MOSFETs and FIN FETs – Phonon Limited Mobility, confinement of acoustic phonons, interface roughness scattering, Coulomb scattering, Temperature dependency of Mobility, High – k Dielectrics

MODULE V

Multi Gate MOSFET Circuit Design: Introduction, Digital circuit design – SRAM Design, Analog circuit design – Operational Amplifier.

Suggestive Reading:

1. FIN FETs and other Multi Gate Transistors, Springer, 2008.
2. Oleg Kononchuk and Bich- Yen Nguyen, Silicon –on – Insulator (SOI) Technology Manufacture and Applications,WP Publishing, 2014.
3. T. Yitterdal , Y. Cheng and T.A. Fjeldly, Device Modeling for Analog and RF CMOS Circuit Design, John Wiley and Sons, 2003.

Course Code	Course Title						Core/ Elective
P21PE015EC	VLSI Testing						Professional Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	3	-	-	-	30	70	3

Course Objectives

1. Describe the VLSI testing philosophy and levels of fault models..
2. Explain about the logic and fault simulation.
3. Illustrate about the Testability measures.
4. Discuss the VLSI Built In Self Test.
5. Illustrate the techniques of Boundary Scan Standard.

Course Outcomes

After completing this course, the student will be able to

1. Understand the basics VLSI testing philosophy and levels of fault models.
2. Analyze deep insight into simulation for design verification and test evaluation.
3. Explore the idea about testability measures.
4. Develop the logic of Built In Self Test.
5. Analyze the system configuration with Boundary Scan.

MODULE I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

MODULE II

Logic And Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

MODULE III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

MODULE IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST

MODULE V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Suggestive Reading:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits” Kluwer Academic Publishers.
2. Parag K. Lala, An Introduction to Logic Circuit Testing, Morgan & Claypool Publishers.
3. Thomas Kropf, Introduction to Formal Hardware Verification, Springer.
4. M. Abramovici, M. A. Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
5. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

Course Code	Course Title						Core/Elective
P21PE016EC	VLSI Physical Design						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Basics of VLSI	3	-	-	-	30	70	3

Course Objectives:

1. Describe basic layers and structure of components like BJTs, MOSFETS.
2. Discuss the layout of basic structures, mask overlays for various structures, problem with device matching and common centroid technique.
3. Illustrate design rules for layout design.
4. Analyze cell based layout design to develop basic gates: NOT, NAND, NOR.
5. Appraise CAD tools to design layout of VLSI circuits.

Course Outcomes:

After completing this course, the student will be able to:

1. Identify the basic structures of MOSFET and understand various layers of VLSI.
2. Interpret the layout of basic structures, mask overlays for various structures, problem with device matching and common centroid technique.
3. Analyze stick diagrams and apply lambda based design rules to draw layout diagrams.
4. Analyze basic cell based layout design and draw the physical design of basic gates, understand the concepts of interconnect delay, floor planning and routing.
5. Employ the CAD tools to design layout of VLSI circuits.

MODULE I

Components of VLSI: Scope of physical design, Components of VLSI, Various layers of VLSI, Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

MODULE II

Basic Concepts of Physical Design: Layout of basic structures wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Mask overlays for different structures. Parasitics, latch up and its prevention. Device matching and common centroid techniques for analog circuits.

MODULE III

Design Rules: Design rules, fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

MODULE IV

Cell concepts: Cell based layout design, Weinberger image array, physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnect delay modeling, floor planning, routing and clock distribution.

MODULE V

CAD Tools: Layout editors, Design rule checkers, circuit extractors, Hierarchical circuit extractors, Automatic layout tools, modelling and extraction of circuit parameters from physical layout. Input-Output Interfacing: Power Supply, Bonding pad, Pad Ring.

Suggested Reading:

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.2012.
2. Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI Design, Third edition.
3. Wayne Wolf, Modern VLSI Design (System-on-Chip), Pearson Education, 3rd Edition 2005.
4. R. Jacob Baker, Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India
5. Preas, M. Lorenzatti, Physical Design and Automation of VLSI Systems, the Benjamin – Cummins Publishers, 1998.

Course Code	Course Title						Core/Elective
P21PC803EC	Real Time Operating Systems Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	2	50	-	1

Course Objectives

1. Demonstrate Task scheduling and task management on ARM microcontroller
2. Understand the concepts of IPC and demonstrate them on ARM Microcontroller
3. Learn the concepts of Real time operating system (VxWorks) and its functions
4. Understand the concept of file system calls and process system calls by programming in UNIX operating system

Course Outcomes

After completing this course, the student will be able to:

1. Comprehend the concepts of RTOS and demonstrate them using ARM microcontroller
2. Simulate the timing concepts and scheduling algorithms using Vx Works
3. Simulate the Message queues and semaphore using Vx Works
4. Understand the concept of file system calls and process system calls by programming in UNIX operating system

List of Experiments:

1. Write a C program to simulate the following non preemptive CPU scheduling algorithms to find "Turnaround time" &"Waiting Time" for: a) FCFS b) SJF c) Round Robin d) Priority Assume all the process arrive at the same time.
2. Simulate Banker's algorithm for Deadlock avoidance.
3. Simulate Banker's algorithm for Deadlock prevention.
4. Simulate the concept of Dining Philosophers problem.
5. Demonstrate the Timing concept of Real Time applications using RTOS on ARM microcontroller kit.
6. To demonstrate the multitasking concept of RT applications using RTOS on ARM.
7. Demonstrate the SEMAPHORE concept of real time application using RTOS on ARM.
8. Demonstrate the MESSAGE QUEUES concept of real time application using RTOS on ARM.
9. Demonstrate the Mail Box concept of real time application using RTOS on ARM.
10. Demonstrate the Round Robin table scheduling using RTOS on ARM.
11. Demonstrate Priority Inversion.
12. Program RS 232 using RTOS.

Course Code	Course Title						Core/Elective
P21PC804EC	Analog Mixed Signal IC Design Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Basics of Analog and Digital Circuits		-	-	-			1

Course Objectives:

1. Observe the response of CMOS logic gates (NOT,NAND,NOR) using Cadence Virtuoso Tools.
2. Analyze the response of CS Amplifiers with Current Mirrors.
3. Simulate and analyze OPAMP based Circuits.
4. Analyze the operation of First order sigma delta modulator.
5. Assess the physical design of CMOS Inverter.

Course Outcomes

After completing this course, the student will be able to:

1. Analyze the response of CMOS logic gates (NOT,NAND,NOR) using Cadence Virtuoso Tools.
2. Simulate and Analyze the response of CS Amplifiers with Current Mirrors.
3. Analyze the responses of Differential Amplifier.
4. Simulate and analyze the responses of OPAMP and its applications.
5. Analyze the Physical design of CMOS Inverter.

List of Experiments

Using Cadence Virtuoso Tools

1. Simulate and verify the MOS O peration and analyze the drain characteristics of MOS Transistors. Also observe its operating point.
2. Design and Simulation of CMOS Inverter, also analyze Transient and DC response of CMOS Inverter and compare its characteristics for different technologies.
3. Analyze the transient response of 2-input CMOS NAND and NOR gates.
4. Simulate and analyze the DC, Transient and AC response of CS Amplifier with basic current mirror.
5. Simulate and analyze the DC, Transient and AC response of CS Amplifier with cascode and Wilson current mirror.
6. Simulate and analyze the DC, Transient and AC response of Differential Amplifier with basic current mirror load.
7. Design and simulate Operational amplifier for the given specifications and analyze its DC, AC and Transient responses. Also measure Its Slew Rate.
8. Design a switched capacitor based Integrator and observe its transient and ac response.
9. Simulate and Analyze the transient and ac response of CMOS Comparator.
10. Design and simulate a first order Sigma –Delta Modulator and analyze its Transient and AC Response, also analyze its Power spectrum.
11. Draw layout of CMOS Inverter and perform DRC, LVS and RC Extraction of CMOS inverter.

Course Code	Course Title						Core/Elective
P21PC805EC	**Mini Project with Seminar**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	4	50	-	2

Course Outcomes

At the end of this course, students will be able to:

1. Formulate a specific problem and give solution
2. Develop model/models either theoretical/practical/numerical form
3. Solve, interpret/correlate the results and discussions
4. Conclude the results obtained
5. Write the documentation in standard format

Guidelines:

- As part of the curriculum in the II- semester of the programme each student shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.
- Each student will be allotted to a faculty supervisor for mentoring.
- Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.
- Mini projects shall have inter-disciplinary/ industry relevance.
- The students can select a mathematical modeling based/Experimental investigations or Numerical modeling
- All the investigations should be clearly stated and documented with the reasons/explanations.
- The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, and detailed discussion on results, conclusions and reference

Departmental committee: Supervisor and a minimum of two faculty members

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 50		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	20	Progress and Review
	05	Report
Departmental Committee	05	Relevance of the Topic
	05	PPT Preparation
	05	Presentation
	05	Question and Answers
	05	Report Preparation

Course Code	Course Title						Core/ Elective
P21PE017EC	MEMS						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	30	70	3

Course Objectives

1. Explain the concept of MEMS technology, materials used and fabrication methods.
2. Differentiate MEMS sensors and actuators based on electrostatic and thermal principles.
3. Illustrate the concept of piezo-electricity and various piezo-electric sensors.
4. Analyze the design of MEMS sensors and actuators for various applications.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the concept of MEMS technology used and fabrication methods.
2. Analyze and differentiate MEMS sensors and actuators based on electrostatic and thermal principles.
3. Interpret the concept of piezo-electricity and various piezo-electric sensors.
4. Analyze the design of MEMS sensors and actuators for various applications.

MODULE I

Micro-Fabrication, Materials And Electromechanical Concepts: Overview of micro fabrication, silicon and other material based fabrication processes, conductivity of semiconductors, crystal planes and orientation, stress and strain, flexural beam bending analysis, torsional deflections, Intrinsic stress, resonant frequency and quality factor, photolithography.

MODULE II

Electrostatic Sensors and Actuation: Principle, material, design and fabrication of parallel plate capacitors as electrostatic sensors, capacitive pressure sensor, and comb drive, micro motors, micro accelerometer for MEMS, Parallel-plate Actuator, Applications**.**

MODULE III

Thermal Sensing and Actuation: Principle, material-design and fabrication of thermocouples, thermal bimorph sensors, thermal resistor sensors, Temperature coefficient of resistance, Thermo-electricity, Thermocouples, Thermal and temperature sensors, heat pump, micro machined thermocouple probe, thermal flow actuators, Applications

MODULE IV

Piezoelectric Sensing and Actuation: Piezo resistance Effect, , Piezo electricity, Piezo resistive Sensor, capacitive sensors, Inductive sensors, MEMS inertial sensors, micro-machined Piezo-electric effect, cantilever piezo electric actuator model, properties of piezo-electric materials, Applications.

MODULE V

Magnetic Sensors: Magnetic material for MEMS, magnetic sensing and detection, manneto resistive sensors, Hall Effect, magneto diode, magneto transistors, MEMS magnetic sensors, RF MEMS.

Case Studies: Acceleration sensors, gyroscopes, magnetic actuation, micro fluids applications, medical applications, optical MEMS.

Suggested Reading:

1. ChangLiu, "Foundations of MEMS", Pearson International Edition,2006.
2. Tai-RanHsu, "MEMS and Micro systems Design and Manufacture", McGrawHill, 2002.
3. Minhang Bao, Analysis and Design Principles of MEMS Devices, ELSEVIER.
4. Stephen Senturia,"Microsystems Design", Springer, 2006.
5. MarcMadou, "Fundamentals of micro fabrication", CRC Press,1997.
6. Boston, "Micromachined Transducers Source book",WCBMcGrawHill,1998.
7. M.H.Bao, "Micro mechanical Transducers: Pressure sensors, accelerometers and gyroscopes", NewYork, 2000.

Course Code	Course Title						Core/Elective
P21PE018EC	Embedded Bio Medical Applications						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Embedded Systems	3	-	-	-	30	70	3

Course Objectives:

1. Describe Low Power Analog circuits like trans-impedance amplifiers, filters and resonators for biomedical systems.
2. Illustrate model for Low Power Bio Medical implants.
3. Examine Bio Medical Electronic Systems.
4. Analyze the Ultra low power Analog and Digital Designs.
5. Describe the Bio Inspired systems like analog vocal tract.

Course Outcomes:

After completing this course, the student will be able to:

1. Understand the basic concepts of Low Power Analog circuits like trans-impedance amplifiers, filters and resonators for biomedical systems.
2. Analyze model for Low Power Bio Medical Systems.
3. Explore Bio Medical Electronic Systems.
4. Analyze the Ultra low power Analog and Digital Designs.
5. Understand and analyze the Bio Inspired systems like analog vocal tract.

MODULE I

Low-Power Analog Biomedical Circuits: Low power trans-impedance amplifiers and photoreceptors - Low power trans-conductance amplifiers and scaling laws for power in analog circuits - Low-power filters and resonators - Low power current - mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system.

MODULE II

Low-Power Biomedical Systems: Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links Low power RF telemetry in biomedical implants - Ultra-low-power implantable medical electronics- cochlear implants or bionic ears - an ultra-low power programmable analog bionic ear processor - low power electrode stimulation - highly miniature electrode - stimulation.

MODULE III

Biomedical Electronic Systems: Brain machine interfaces for the blind - Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power non-invasive medical electronics - switched-capacitor model of the heart - micro-power electrocardiogram amplifier - Low-power pulse oximetry - Battery-free tags for body sensor networks - Intra-body galvanic communication networks - Biomolecular sensing.

MODULE IV

Principles for Ultra-Low-Power Analog and Digital Design: Digital design: Sizing and topologies for robust sub threshold operation - power dissipation - energy efficiency Optimization - Varying power supply voltage and threshold voltage - gated clocks - Basics of adiabatic computing - Architectures and algorithms for improving energy efficiency. Analog and mixed-signal design: Power consumption in analog and digital systems - optimum point for digitization in a mixed-signal system - The Shannon limit for energy efficiency Collective analog or hybrid computation - HSMs: general-purpose mixed-signal systems with feedback - General principles for low-power mixed-signal system

design - Actuators and sensors.

MODULE V

Bio-Inspired Systems: Neuromorphic electronics - RF-cochlea design - bio-inspired analog vocal tract - vision architectures - Spike-based hybrid computers - Energy efficiency Cytomorphic electronics: cell-inspired electronics - Electronic analogies of chemical reactions - Log-domain current-mode models of chemical reactions and protein-protein networks - Analog circuit models of gene-protein dynamics - gene-protein circuits - Hybrid analog-digital computation in cells, neurons and brain.

Suggested Reading:

1. Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems", Cambridge University Press, 2011.
2. Kris Iniewski, "VLSI Circuit Design for Biomedical Applications", Artech House Publishers, 2008.
3. Tan Nianxiong Nick, Li Dongmei, Wang Zhihua, "Ultra Low Power Integrated Circuit Design: Circuits, Systems, and Applications", Springer Publications, 2014.
4. Mead, "Analog VLSI and Neural Systems", Addison Wesley Publishing Company, 1990.

Course Code	Course Title						Core/ Elective
P21PE019EC	VLSI Architectures						Elective
	Contact Hours per Week						
Prerequisite	L	T	D	P	CIE	SEE	Credits
VLSI Design	3	-	-	-	30	70	3

Course Objectives:

1. Describe the basics of different processors including architecture and organization
2. Analyze the ability of handling and designing different types of pipe lining techniques.
3. Discuss various memory organization and management techniques
4. Illustrate array architecture for DSP and analyze Field Programmable Analog Array architecture.
5. Explain dynamic reconfiguration and analyze the performance of dynamically reconfigurable systems.

Course outcomes:

After completing this course, the student will be able to:

1. Review the basics of different processors including architecture and organization
2. Foster ability of handling and designing different types of pipe lining techniques.
3. Understand various memory organization and management techniques
4. Analyze the various advanced architectures.
5. Familiarize with the parallel, shared architectures and important organizational

MODULE I

Introduction: Review of VLSI Design flow. Goals of VLSI Design: Optimization of speed, power dissipation, cost and reliability.

Algorithm to architecture transformation: Architectural antipodes, transform approach to VLSI architectures, graph based formalism for describing processing algorithms, isomorphic architecture.

Equivalence transforms for combinational computations: Common assumptions, pipelining, replication, time sharing, associatively transform and other algebraic transforms.

MODULE II

Architectural Synthesis and Optimization: Circuit specifications for architectural synthesis, fundamental architectural synthesis problems, temporal domain-scheduling, spatial domain binding, sequencing graphs, hierarchical models, synchronization problem, area and performance estimation, data path and control unit synthesis, constrained and unconstrained scheduling, scheduling of pipelined circuits.

MODULE III

Clocking of synchronous circuits: Single-phase and two-phase clocking, wave pipelining, collective clock buffer design, distributed clock buffer trees, hybrid clock distribution networks, and impact of clock distribution delay on I/O timing.

Asynchronous data processing architectures: Data consistency problem of vectored acquisition-plain bit parallel synchronization, unit distance coding, suppression of cross patterns, handshaking, partial handshaking, data consistency problem of scalar acquisition-synchronization at single place, synchronization at multiple places, synchronization from a slow clock, meta stable synchronizer behavior.

MODULE IV

Digital Signal Processing using array architectures: Systolic and wave-front arrays, mapping dependence and signal flow graphs to systolic and wave-front arrays, asynchronous communication protocols for wave-front arrays.

Analog array architectures: Architectural design of field programmable analog array (FPAA), design of switched capacitor and pulsed mode FPAA, scalability of FPAA.

MODULE V

Dynamically reconfigurable gate arrays: Static versus dynamic reconfiguration, single context versus multi-context dynamic reconfiguration, full versus partial run time reconfiguration, performance analysis of dynamically reconfigurable systems.

Inexact computing systems: Probabilistic CMOS model based architectures and probabilistic pruning.

Suggested Reading:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press (2009).
2. Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, McGraw Hill (2012).
3. S.Y. Kung, “VLSI Array Processors”, Prentice Hall (2012).
4. A.M. Fahim, “Clock generators for SoC processors: Circuits and Architectures”, Kluwer Academic Publishers (2005).
5. Magdy A. Bayoumi, “VLSI Design Methodologies for Digital Signal Processing Architectures”, Springer (2012).

Course Code	Course Title						Core/ Elective
P21PE020EC	Machine Learning with Artificial Neural Networks						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	30	70	3

Course Objectives

1. Discuss the basic theory underlying machine learning.
2. Illustrate the importance of dimensionality reduction and clustering methods.
3. Analyze the SVM for classification and concept of neural network.
4. Describe the architecture, issues of various feed forward and feedback neural networks.
5. Compare different neural network architectures and select the appropriate architecture for a given problem.

Course Outcomes

After completing this course, the student will be able to:

1. Understand the basic theory underlying machine learning
2. Explore the methods of dimensionality reduction and clustering
3. Familiarize SVM for classification problem and understand basic Neural Network
4. Evaluate weight gradients in a feed forward neural network by using the back propagation algorithm.
5. Apply learning rules to perform the training with appropriate neural networks.

MODULE I

Introduction: Definitions, Datasets for Machine Learning, Different Paradigms of Machine Learning, Data Normalization, Hypothesis Evaluation, Linear Regression. Parameter Estimation: Maximum Likelihood and Bayesian Parameter Estimation

MODULE II

Feature Selection and Dimensionality Reduction: Principal Component Analysis (Eigen values, Eigen vectors, Orthogonality), Linear Discriminate Analysis. Clustering: Distance measures, Different clustering methods (Distance, Density, Hierarchical), Types of clustering algorithms: k-means clustering, Hierarchical Clustering Algorithm**.**

MODULE III

Classification: Support Vector Machines, Linear learning machines and Kernel space, Making Kernels and working in feature space, Implementation of SVM for classification and regression problems.
Artificial Neural Networks: Introduction and ANN Structure: Biological neurons and artificial neurons. Model of an ANN, Activation functions used in ANNs. Typical classes of network architectures: Multilayer Perception. Software implementation of various activation functions.

MODULE IV

Back propagation: Training and Convergence, Radial Basis Functions-Net, Feed Forward ANN: Structures of Multi-layer Feed Forward Networks.
Training Neural Networks: Loss, Training/Validating/Testing, Optimization: Gradient Descent, Stochastic Gradient Descent, ADAM, Overfitting: Drop out, Normalization. Training Neural Networks with various activation function and optimization using MatLab/Keras/ any suitable software.

MODULE V

Convolutional Neural Networks: Motivation (Neuroscience), Convolutional layers, Additional layers, Training CNN, Classification examples (AlexNet) with MatLab/Keras/ any suitable software.
Recurrent Neural Networks: Training RNNs with MatLab/Keras/ any suitable software.
Adversarial Approaches to ANN / Generative Adversarial Neural Networks: Training GANs with MatLab/Keras/ any suitable software.

Suggested Reading:

1. Tom Michel, Machine Learning, McGraw Hill, 1997
2. B. Yeganaranarana, Artificial Neural Networks, Prentice Hall, New Delhi, 2007.
3. M. Gopal, Applied Machine Learning, McGraw Hill Education (India).
4. Simon Haykin, Neural Networks (A Comprehensive Foundation), McMillan College Publishing Company, New York, 1994.
5. Salman Khan, Hossein Rahmani, Syed Afaq Ali Shah, Mohammed Bennamoun , A Guide to Convolutional Neural Networks for Computer Vision, Morgan & Claypool Publishers, 2018.

Course Code	Course Title						Core / Elective
P21OE003EC	Fundamentals of Embedded System Design						Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Microcontrollers	3	-	-		30	75	3

Course Objectives

1. Discuss embedded system architectures, challenges and design issues.
2. Describe PIC microcontroller, its features and programming.
3. Illustrate ARM Microcontroller architectural details and instruction set.
4. Explain ARM Memory management.
5. Explore the embedded software tools to develop an embedded system.

Course Outcomes

1. Understand embedded system architectures, challenges and design issues.
2. Explain PIC microcontroller, its features and programming.
3. Analyze ARM Microcontroller architectural details and instruction set.
4. Understand ARM Memory management.
5. Apply the embedded software tools to develop an embedded system.

MODULE I

Introduction to Embedded Systems: Overview of Embedded System Architecture, Challenges & Trends of Embedded Systems, Hardware Architecture, Software Architecture. Application areas of Embedded Systems & Categories of Embedded Systems. Embedded System Design & Co-Design issues and Design Cycle Process.

MODULE II

PIC 18: Family Overview, Architecture, Instruction Set, Addressing modes. Timers and Interrupts of PIC 18 and Capture/Compare and PWM modules of PIC 18.

MODULE III

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

MODULE IV

ARM Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instruction Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Exception and interrupt handling.

ARM Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation Access Permissions, Context Switch.

MODULE V

Embedded Software Development Tools: Embedded Software Development Tools, Host and Target Machines, Linkers/Locators for Embedded Software, Getting Embedded Software into the Target System. Debugging Techniques.

Suggested Reading:

1. Raj Kamal, "Embedded Systems – Architecture, Programming and Design", 2nd Edition, TMH, 2008.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guides – Designing & Optimizing System Software", Elsevier, 2008.
3. Mazidi, MCKinlay and Danny Causey, "PIC Microcontrollers and Embedded Systems", Pearson Education, 2007
4. David.E.Simon, "An Embedded Software Primer," 1st Edition, Pearson Education, 1999.
5. Jonathan W. Valvano, "Embedded Microcomputer Systems, Real Time Interfacing", Thomas Learning, 1999.

Course Code	Course Title						Core/Elective
PC 3356 EV	Major Project Phase — I						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	20	100	-	10

Course Outcomes

At the end of this course, students will be able to:

1. Exposed to self-learning various topics.
2. Learn to survey the literature such as books, journals and contact resource persons for the selected topic of research.
3. Learn to write technical reports.
4. Develop oral and written communication skills to present.
5. Defend their work in front of technically qualified audience

Guidelines:

a) The abstract presentation to be made after discussing with the supervisor allotted.

b) The title of the project work will be chosen after literature review. The papers selected for literature review are to be from reputed journals only (Like IEEE, SCOPUS etc). The number of papers to be reviewed must be a minimum of 25.

c) A presentation of the abstract has to be made by the student in front of the committee (constituted by the Head of the Department) must consist of the following:

i. Title of the project work

ii. Area of the project work

iii. List of papers reviewed in *IEEE format (minimum papers to be reviewed are 25)

iv. A review paper closest to the proposed project work may be identified.

d) Title of the project work & area of the project work cannot be modified once finalized.

e) The student must meet the supervisor allotted at least once in two weeks to appraise the progress of the project work. The supervisor will review the progress of the project work and present his/ her remarks on the progress made.

f) The report must consist of detailed problem statement, literature reviews & preliminary results in Major Project Phase –I.

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	30	Project Status / Review(s)
	20	Report
Departmental Committee(Chairperson BOS, Osmania University and Head, Supervisor& Project Coordinator from the respective department of the institution.	10	Relevance of the Topic
	10	PPT Preparation
	10	Presentation
	10	Question and Answers
	10	Report Preparation

Not Note: The Supervisor has to assess the progress of the student regularly.

Course Code	Course Title						Core/Elective
	Major Project Phase H (Dissertation)						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	-	-	-	32	-	200	16

Course Outcomes

At the end of this course, students will be able to:

1. Use different experimental techniques and will be able to use different software/ analytical tools.
2. Design and develop an experimental set up/ equipment/test rig.
3. Conduct tests on existing set ups/equipments and draw logical conclusions from the results after analysing them.
4. Either work in a research environment or in an industrial environment.
5. Conversant with technical report writing and will be able to present and convince their topic of study to the engineering community.

Guidelines:

- It is a continuation of Major Project Phase — I started in semester - III.
- The student has to submit the report in prescribed format and also present a seminar.
- The dissertation should be presented in standard format as provided by the department.
- The candidate has to prepare a detailed project report consisting of introduction of the problem, problem statement, literature review, objectives of the work, methodology (experimental set up or numerical details as the case may be) of solution and results and discussion.
- The report must bring out the conclusions of the work and future scope for the study. The work has to be presented in front of the examiners panel consisting of an approved external examiner and Chairperson BoS, & Head, Osmania University and Supervisor from the Institute.
- The candidate has to be in regular contact with his/her Supervisor / Co- Supervisor

Guidelines for awarding marks in SEE (Semester End Examination): Max. Marks: 200		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	30	Quality of the work which may lead to
	10	Analytical / Programming / Experimental Skills Preparation
	10	Report preparation in a standard format
External Examiner and Chairperson, Bos & Head, Osmania University (All together)	20	Power Point Presentation
	60	Quality of thesis and evaluation
	30	Innovations, application to society and Scope for future study
	20	Viva-Voce